

Large-Signal Microwave Characterization of AlGaAs/GaAs HBT's Based on a Physics-Based Electrothermal Model

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Abstract—A physics-based multicell electrothermal equivalent circuit model is described that is applied to the large-signal microwave characterization of AlGaAs/GaAs HBT's. This highly efficient model, which incorporates a new multifinger electrothermal model, has been used to perform dc, small-signal and load-pull characterization, and investigate parameter-spreads due to fabrication process variations. An enhanced Newton algorithm is presented for solving the nonlinear system of equations for the model and associated circuit simulator, which allows a faster and more robust solution than contemporary quasi-Newton nonlinear schemes. The model has been applied to the characterization of heterojunction bipolar transistor (HBT) microwave power amplifiers.

I. INTRODUCTION

HETEROJUNCTION bipolar transistors (HBT's) have demonstrated high-power output densities at microwave frequencies and are increasingly being utilized for large-signal applications such as power amplifiers, oscillators, and mixers [1]–[3]. The design of these circuits is challenging because of their nonlinear behavior and accurate large-signal models are required to expedite this process. In the case of HBT's, the high power densities associated with these devices can lead to significant operating temperatures when the transistor is used in large-signal applications. Although the temperature sensitivity of transistor parameters is significant for all types of power transistors, it is particularly important for the HBT with its high associated power densities, relatively poor thermal conductivity, and strong dependence of junction behavior on temperature. This means that it is essential to characterize the large-signal model of the HBT as a function of operating and ambient temperatures in order to obtain an accurate model for CAD. Finally, there are a number of advantages in relating the operation of the device to the structure and transport properties of the transistor. In particular, this allows the design of the device to be optimized for a particular application, and the model can be used to predict the parameter spreads for a particular design and fabrication process. In the case of power transistors, with many emitter fingers distributed throughout a repeating cell structure (Fig. 1), it is desirable to model the electrical and thermal aspects of individual cells, which may vary across the structure. This generally requires a physical model.

Detailed two-dimensional (2-D) physical models, which solve a set of transport equations have been reported (for example [4], [5]) and provide a valuable insight in to the physics behind the operation of HBT's. However, there are a number of issues that still need to be addressed to obtain good quantitative correlation between these physical models and measured data (including hot electron effects, representation of hetero-transport properties, processing dependent junction ideality factors and saturation currents). Furthermore, although these models are suitable for modern workstations, they still require substantial computation time to execute single bias point simulations and are unsuitable for microwave computer-aided-design. An attractive alternative that combines some of the advantages of physical models with the relative simplicity of implementation of equivalent circuit models is found in physics-based models, where the element values can be related to the structure and semiconductor properties of the device.

This paper describes a physics-based multicell electrothermal HBT model, Fig. 2, which can be used to predict the performance of the transistor for dc, small- and large-signal modes of operation. It is suited to process-oriented design. The model has been integrated into a harmonic-balance simulator to perform simulated load-pull characterization of power transistors. The results obtained from this analysis are compared with measured data obtained for prototype devices. An enhanced Newton algorithm is presented which allows very rapid convergence of the nonlinear solution algorithm compared with contemporary modified-Newton schemes. Finally, a novel multifinger coupled electrothermal model based on a thermal resistance matrix concept is described that accounts for local heating and thermal runaway effects.

II. PHYSICS-BASED EQUIVALENT CIRCUIT MODEL

A number of large-signal equivalent circuit HBT models have been described in the literature [6]–[9], including notable examples of physics-based models and modified SPICE bipolar transistor models [10]. However, few of these have accounted for the process-dependent nature of the transistor and require extensive microwave and dc data to extract the element values. In other cases the complexity of the model leads to difficulties in obtaining fully converged solutions from the nonlinear solver and additional convergence problems when used in association with harmonic-balance algorithms.

Ebers–Moll representations have been produced for microwave HBT's ([11], [12] are good examples), but they are

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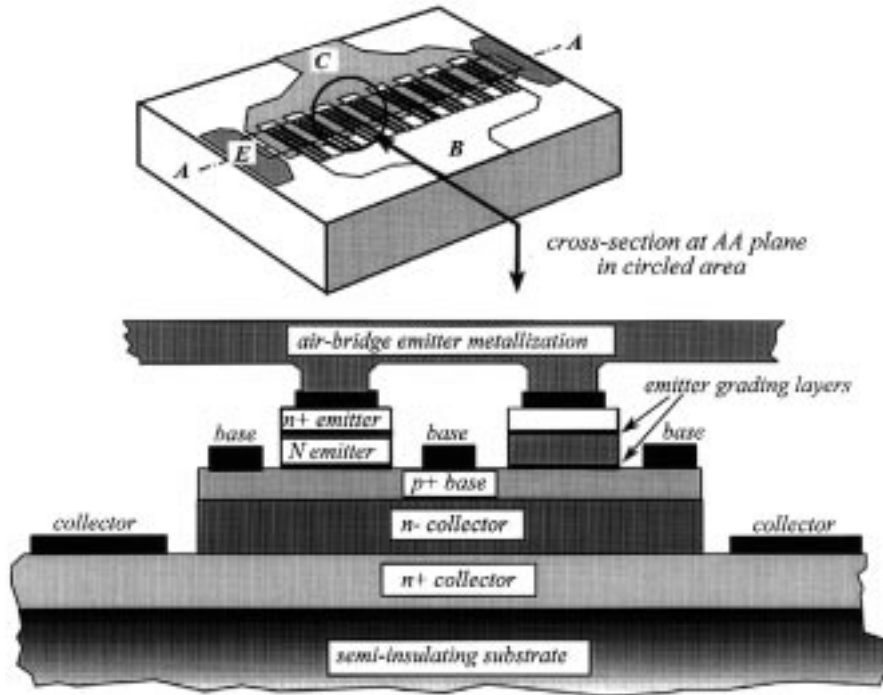


Fig. 1. Schematic view of a typical multicell power HBT chip structure with detail cross section of one cell containing two emitter fingers (data from the cross section forms the basis of the physics-based description).

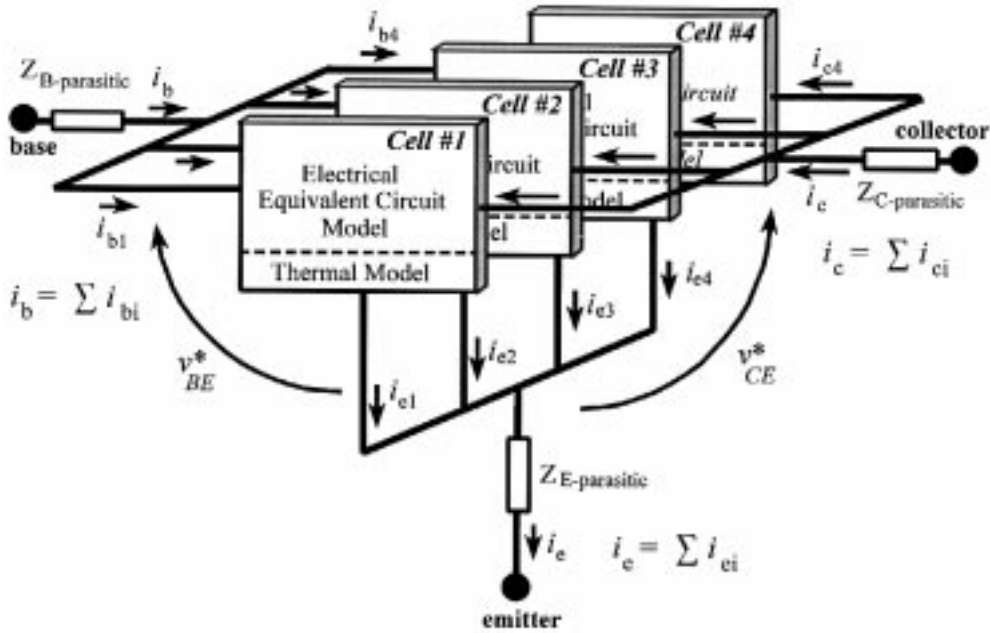


Fig. 2. Multicell electrothermal model for a HBT, illustrating coupling of cells and self-consistent solution of 1) electrical and thermal equivalent circuit models inside each cell and 2) entire device. Each cell corresponds to a section of the transistor associated with a single emitter finger (four cells illustrated here). The notation v_{BE}^* and v_{CE}^* indicate the voltages across the terminals of each cell.

usually empirical in nature and are again difficult to relate to device structure and material parameters. The Gummel-Poon model, which is essentially a charge-control model, provides a superior representation in terms of the physical operation compared with the basic Ebers-Moll model, remaining valid in the high injection regime and including recombination effects present in the space-charge regions. However, the basic Gummel-Poon model it is not directly applicable to HBT's,

because the base current in HBT's is dominated by surface or junction space charge region (SCR) recombination, rather than hole injection from the base into the emitter as in BJT's. Furthermore, the base current at low current densities is mainly due to surface recombination [13], [14]. The temperature dependence of the equivalent circuit element values suggests that the base current at high current densities is largely attributable to SCR recombination. A consequence of this is

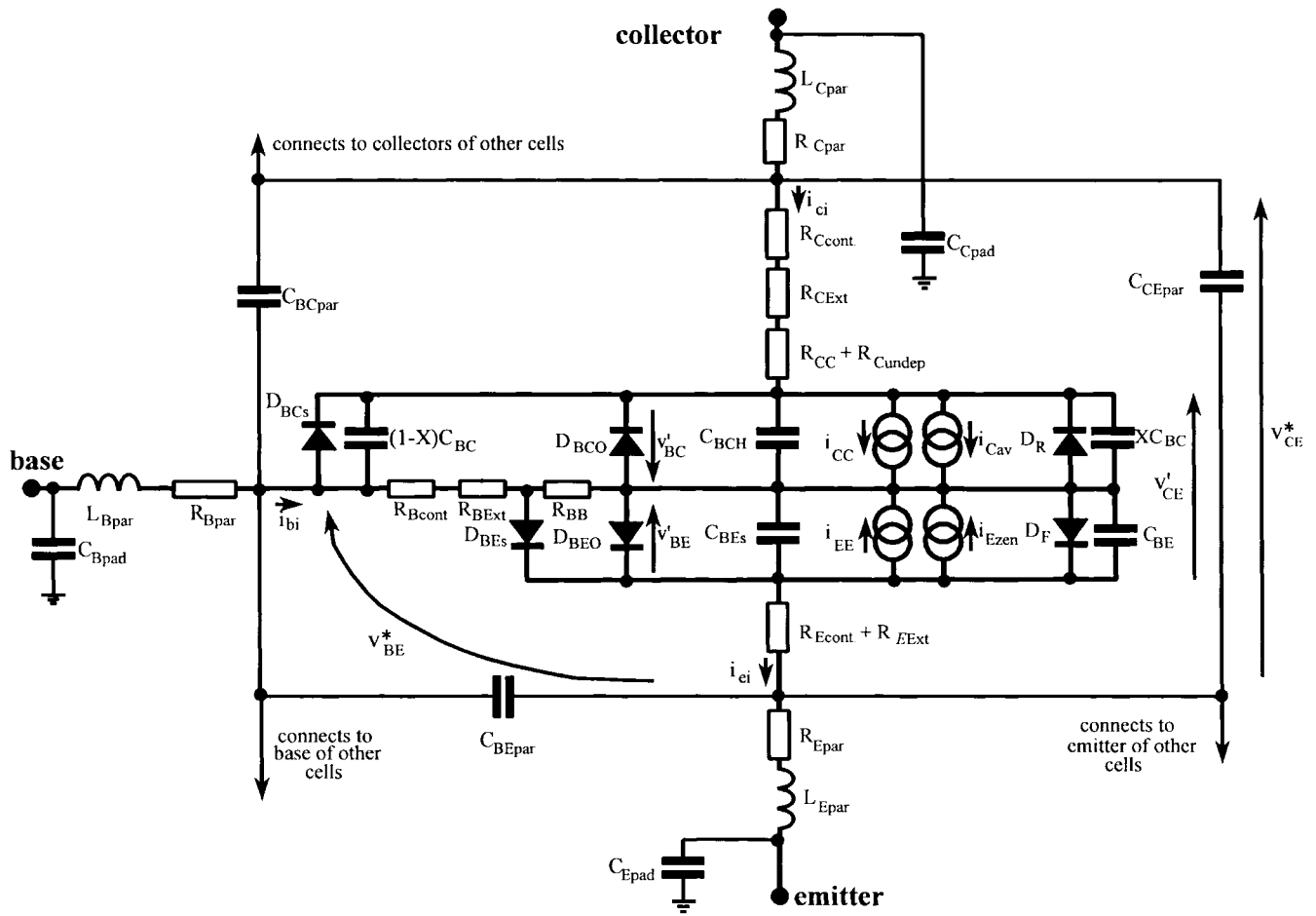


Fig. 3. Physics-based dc and large-signal equivalent circuit model of one cell of the HBT model.

that the ideality factor of the base current is always higher than the ideality factor of the collector current. This results in two regions of increasing current gain in the HBT, defined by the component of base current that is dominant in each region (surface or bulk recombination). This contrasts with the classical Gummel–Poon model, where the current gain increases initially, flattens, and then decreases with increasing V_{BE} .

On the basis of investigations performed using 2-D numerical models, it was found appropriate during the development of the model described here to neglect hole injection into the emitter from the base; recombination through deep levels in the base–emitter space–charge region; hole injection into the collector from the base; and recombination through deep levels in the base–collector space charge region. Emitter crowding is negligible in HBT's, unlike the situation in BJT's. This results in a useful simplification of the model without compromising the accuracy from the point of view of microwave CAD.

The electrical equivalent circuit model of one emitter “cell” of an HBT, developed during this work is shown in Fig. 3, and can be considered in terms of forward and reverse current components. This diagram shows the six ideal diodes which describe the behavior of the transistor junctions. The forward and reverse base current has two components—the SCR recombination (described by I_{SE}, N_E and I_{SC}, N_C for D_{BE0} and D_{BC0} , respectively) and the surface recombination (described by I_{SES}, N_{ES} and I_{SCS}, N_{CS} for D_{BES} and D_{BCS} ,

respectively). The electron injection into the base from the emitter is modeled by the diode D_F (I_{SF}, N_F) and the electron injection into the base from the collector by the diode D_R (I_{SR}, N_R). This arrangement of six diodes allows the diode parameters to assume physically meaningful values across the full range of bias conditions in contrast to HBT models utilizing four diodes. The latter cannot satisfactorily model surface recombination and often lead to compromised fits to Gummel data, when the full range of currents are considered. The electron injection into the base is characterized by ideality factors close to unity (N_F and N_R). The surface recombination components typically have ideality factors in the region of 1.6 to 2 (N_{ES} and N_{CS}). The thermal voltage $V_{Ti}(kT_i/q)$ in the diode equations (Table I) reflects the temperature T_i of the individual cell i , associated with the diodes in the model for each cell. Note that the diode currents are functions of the intrinsic base–emitter and base–collector voltages v'_{BE} and v'_{BC} , respectively, of each cell.

The saturation currents and ideality factors associated with the ideal diodes that model the junctions are very sensitive to processing conditions and have proven difficult to unambiguously extract from physical models, although recently reported results indicate that such an extraction is feasible [15]. Forward and reverse Gummel plots ($\log(I)/V$) [16] are used to determine the diode parameters, shown in Table I. The temperature of the transistor must be accurately determined and

maintained during the duration of the measurement. If accurate temperature measurement is not possible, the average device temperature T can be estimated by assuming an idealized exponential characteristic for the base–collector junction (where N_R is assumed to be unity), when the device is operating in the reverse mode ($\exp(V_{BC}/V_T)$). The average device temperature can be extracted from the reverse characteristics using $T = (q/k)[\partial V_{BC}/\partial \ln(I_E)]$. A constant device temperature can be achieved using a pulse-measurement capability to avoid self-heating, with the device held in a temperature stabilized environment (such as a temperature controlled oven or probe-station stage). The saturation current I_S can be obtained by determining the intercept of the $\log(I)$ axis, corresponding to $V_B = 0$ V, and the ideality factor N is determined from the gradient of the collector current characteristic using $N = 1/(\text{gradient} \cdot \ln(10) \cdot V_T)$. A typical measured forward Gummel plot of an AlGaAs/GaAs HBT is shown in Fig. 4. The deviation in IC at low current levels is due to limited sensitivity in the measurement system. At high current levels the characteristics bend principally as a consequence of voltage dropped across the base and emitter resistances. One of the difficulties encountered in extracting the saturation currents and ideality factors from measured data is the sensitivity to the “choice” of line used to approximate the characteristic if a manual estimation is made by simple inspection. A superior method of determining these values is to use singular value decomposition (SVD) in association with a least squares fit. The SVD method of extracting HBT parameters was used by Hafizi *et al.* [14], who developed an iterative least squares fitting technique to extract the transistor diode and current gain parameters. A singular value decomposition (SVD) matrix factorization technique [14], [17], is used in this work. This approach ensures that linear dependence among the basis functions and limited machine and data accuracy have a minimal adverse effect on the quality of fit achieved. The problem of bending in the Gummel plots at high current levels and the associated problem of obtaining a suitable linear approximation to find I_S and N_F , can be overcome by plotting $\log(\beta)$ against $\log(I_c)$ [18]. The use of $\log(I_c)$ as the independent variable corresponds with the use of the intrinsic base–emitter voltage V'_{BE} , because the high doping in the base of HBT's eliminates high injection effects. The parameters I_{SE} , N_E , I_{SES} , and N_{ES} can be obtained using the $\log(\beta)/\log(I_c)$ characteristics as described in [10] and [18]. Again the SVD least squares algorithm is preferred here to minimize errors. The quality of fit to measured data is shown in Fig. 4 and the associated parameters for a typical power HBT are shown in Table I (the chi-square test for the fit is typically better than 10^{-3} for all diode parameters). It is important to appreciate at this stage that after the initial fit to Gummel data and extraction of parasitic element values (usually determined during microwave calibration), no further fitting is carried out and the measured data is compared directly with the predicted simulation results in the remainder of this paper.

The saturation currents (I_{SE} , I_{SES} , I_{SC} , I_{SCS} , I_S , I_{SR}) are assumed to have a simplified temperature dependence of the

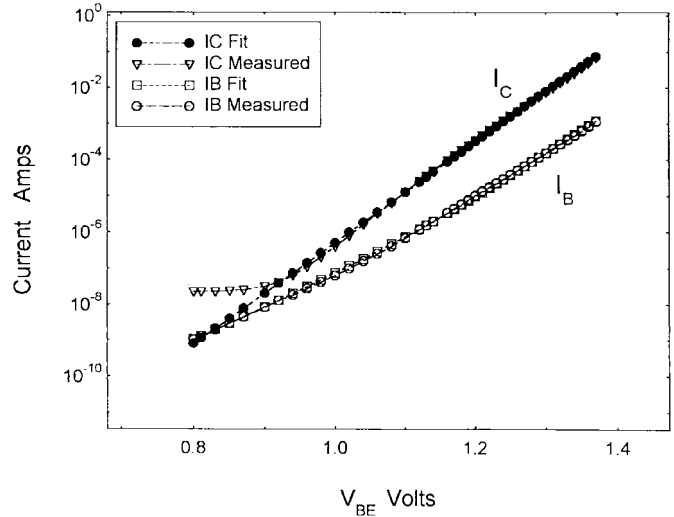


Fig. 4. Forward Gummel plots for an AlGaAs/GaAs HBT showing measured and fitted data (SVD algorithms and a six-diode model were used to obtain a high quality fit).

form [10]:

$$\ln(I_S) = \frac{-T_S}{T} + \ln(I_{S0}) \quad (1)$$

where T is the temperature in Kelvin. T_S and I_{S0} are constants that define the temperature dependence of the saturation current. The values of T_S and I_{S0} are extracted from plots of $\log(\text{saturation current})$ against $1/T$ by fitting a straight line to measured data. The temperature coefficients of the saturation currents are also be extracted using the SVD least-squares fitting algorithm, when more than two sets of data points are available. In the case of temperature dependent ideality factors, the ideality factor is approximated using a temperature dependence as follows:

$$N(T) = N_S(T=0)[1 + \alpha\Delta T]. \quad (2)$$

Here, the ideality factor N_S is referenced to $T = 0$ K. The temperature coefficient of the saturation current and ideality factors require data taken from at least three different die temperatures. This can be obtained from measured data or extracted using thermal simulations of the type described later in this paper.

The current sources in the model represent the four processes of base transport, collection of injected electrons, base–collector avalanche breakdown, and base–emitter zener breakdown. The recombination processes in the base are modeled using time-dependent electron collection current sources i_{CC} and i_{EE} (Table I). A fraction α_T of the injected electron current I_F is collected by the collector (the parameter α_T is the base transport factor, which in an ideal device with no recombination would be unity). The model (Table I) utilizes the forward Early voltage V_{AF} and reverse Early voltage V_{AR} , both of which assume high values in HBT's. Most of the current source parameters are defined on the basis of the transport and physics of the device (see Table I).

Velocity overshoot can have a significant effect on the transport of carriers in HBT's and plays a significant role in

TABLE I
FUNCTIONAL FORMS AND TYPICAL PARAMETER VALUES FOR DIODES AND CURRENT SOURCES
FOR THE PHYSICS-BASED MODEL OF A $16 \times 3 \times 20 \mu\text{m}$ (16-EMITTER FINGER) TRANSISTOR

Model Element	Description and comments	Functional Form	Typical parameter values per cell for $16 \times 3 \times 20 \mu\text{m}$ emitter HBT (2 emitter fing./cell)
D_F	Electron injection from emitter to base	$I_F(t) = I_{SF} \left[\exp \left(\frac{v_{BE}(t)}{N_F V_{T_i}} \right) - 1 \right]$ Note: individual cell temperature T_i used to calculate V_{T_i}	$J_{SF0} = 2.65 \times 10^{11} \text{ Am}^{-2}$ $T_{SF0} = 18,450 \text{ K}$ $N_F(0) = 1.028$ $\alpha_F = 0.0 \text{ K}^{-1}$
D_R	Electron injection from collector to base	Functional form as D_F , with $I_R(t)$, I_{SR} , v'_{BC} and N_R	$J_{SR0} = 7.33 \times 10^{10} \text{ Am}^{-2}$ $T_{SR0} = 18,520 \text{ K}$ $N_R(0) = 1.002$ $\alpha_F = 0.0 \text{ K}^{-1}$
D_{BEO}	Optical recombination in the B-E space charge region.	Functional form as D_F , with $I_{BEO}(t)$, I_{SE} , v'_{BE} and N_E	$J_{SE0} = 1.62 \times 10^{10} \text{ Am}^{-2}$ $T_{SE0} = 18,600 \text{ K}$ $N_E(0) = 1.036$ $\alpha_{BEO} = 7 \times 10^{-4} \text{ K}^{-1}$
D_{BCO}	Optical recombination in the B-C space charge region.	Functional form as D_F , with $I_{BCO}(t)$, I_{SC} , v'_{BC} and N_C . (comment: negligible)	$J_{SC0} = 4.00 \times 10^{18} \text{ Am}^{-2}$ $T_{SC0} = 18,400 \text{ K}$ $N_C(0) = 1.656$ $\alpha_{BEO} = 2 \times 10^{-6} \text{ K}^{-1}$
D_{BEs}	Base-emitter surface recombination.	Functional form as D_F , with $I_{BES}(t)$, I_{SEs} , v'_{BE} and N_{ES}	$J_{SEs0} = 9.19 \times 10^{-02} \text{ A/m}$ $T_{SEs0} = 9760 \text{ K}$ $N_{ES}(0) = 1.663$ $\alpha_{BEs} = -1 \times 10^{-3} \text{ K}^{-1}$
D_{BCs}	Base-collector surface recombination.	Functional form as D_F , with $I_{BCS}(t)$, I_{SCs} , v'_{BC} and N_{CS}	$J_{SCs0} = 8.10 \times 10^{-18} \text{ A/m}$ $T_{SCs0} = 9740 \text{ K}$ $N_{CS}(0) = 1.910$ $\alpha_{BCs} = -1 \times 10^{-6} \text{ K}^{-1}$
i_{CC} , i_{EE}	Collected electron currents (i_{EE} is similar in functional form to i_{CC} , shown here for brevity) w_C - thickness collector depletion region w_B - thickness of base region	$i_{CC} = \frac{1}{w_C} \left(v_{ov} \int_{t-\tau_B-\tau_{ov}}^{t-\tau_B} I_{Cz}(\tau) d\tau + v_{sat} \int_{t-\tau_B-\tau_C}^{t-\tau_B-\tau_{ov}} I_{Cz}(\tau) d\tau \right)$ $I_{Cz}(\tau) = \alpha_T I_{SF} \left(1 - \frac{v_{BC}(\tau \cdot \tau_B)}{V_{AF}} \right) \left(\exp \left(\frac{v_{BE}(\tau)}{N_F V_{T_i}} \right) - 1 \right)$ $\alpha_T \approx 1 - 0.5 \left(\frac{w_B}{L_{BD}} \right)^2 \quad \text{if } L_{BD} \gg w_B$	$v_{ov} = 3 \times 10^5 \text{ ms}^{-1}$ $v_{sat} = 1 \times 10^5 \text{ ms}^{-1}$ $\tau_{ov} = 1 \text{ ps}$ $\tau_B = 0.9 \text{ ps}$ $\tau_C = 3.5 \text{ ps}$ $w_C = 0.5 \mu\text{m}$ $V_{AF} = 1500 \text{ V}$ $w_B = 0.1 \mu\text{m}$ $L_{BD} = 0.8 \mu\text{m}$
i_{Cav} , i_{Ezm}	Collector avalanche breakdown i_{Cav} for a given base-collector breakdown voltage V_{BCBO} . (Emitter zener breakdown is modelled in a similar fashion for V_{BEB})	$i_{Cav} = i_{cc}(t) \cdot (24.4602 \zeta^2 - 212.838 \zeta^3 + 1003.66 \zeta^4 - 2649.26 \zeta^5 + 3993.69 \zeta^6 - 3202.85 \zeta^7 + 1067.62 \zeta^8)$ where $\zeta = (V_{CB} / V_{BCBO})^{N_{Cav}}$ with $V_{BCBO} = V_{CBO}(T_A)(1 + \alpha_{Cav} \Delta T)$ $\zeta_{BCBO} \approx E_{max} w_{coll} - \frac{q N_{Dcoll} w_{coll}^2}{2.0 \epsilon} \quad \text{abrupt junction}$ $V_{BEB} = E_z^2 \epsilon (N_{Abase} N_{Demitter}) / (2.0 q N_{Abase} N_{Demitter})$	$V_{BCBO} = 18.5 \text{ V}$ ($T_A = 40^\circ \text{C}$) $N_{Cav} = 4.1$ $\alpha_{Cav} = 7 \times 10^{-4} \text{ K}^{-1}$ $V_{BEB} = 12 \text{ V}$ ($T_z = 40^\circ \text{C}$) $N_{Ezm} = 5.0$ $\alpha_{Ezm} = -9 \times 10^{-4} \text{ K}^{-1}$ E_{max} and E_z are doping dependent breakdown fields.

the base-collector space-charge region [10], [12], [19]. An approach similar to that of Grossman *et al.* [10] has been adopted here, where the current i_{CC} in the base-collector space-charge region is calculated using a simplified two-section velocity profile. The two velocities, v_{OV} and v_{SAT} correspond to the average velocity in the overshoot region and the average velocity in the saturated region, respectively,

(taken here as $3 \times 10^5 \text{ ms}^{-1}$ and $1 \times 10^5 \text{ ms}^{-1}$, respectively, for n -type GaAs). The current i_{EE} is evaluated in a similar manner to i_{CC} .

The bulk ohmic resistances R_{BExt} , R_{CEExt} , R_{EEExt} , vertical contact resistance R_{Econt} , lateral contact resistances R_{Bcont} , R_{Ccont} , and spreading resistance spreading resistances R_{BB} , R_{CC} , and the resistance of the undepleted collector

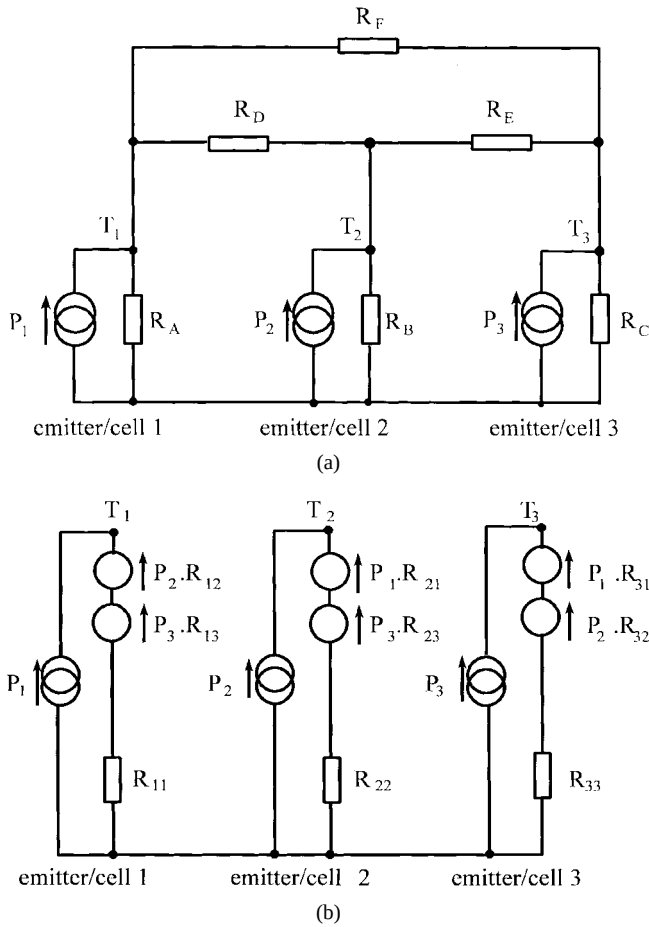


Fig. 5. Multicell thermal equivalent circuits of a three-emitter finger HBT. (a) Conventional model. (b) Model based on thermal resistance matrix method.

region R_{Cundep} , are defined using the established physical descriptions (see, for example, [10], [20], [21]). The model is simplified by neglecting the vertical base contact resistance, intrinsic vertical bulk ohmic base resistance, and the intrinsic emitter vertical resistance, which assume very small values in practice compared with the other associated resistances.

The capacitances associated with HBT's have been modeled using well-known physical depletion region approximations and space-charge region charge-storage relationships described in [10], [20], and [21], taking full account of the graded heterojunction at the emitter (C_{BE} and C_{BEs}). The base-collector junction in most HBT's is an abrupt homojunction, consisting of the highly doped base and lightly doped collector regions, Fig. 4. The lightly doped collector region interfaces with the highly doped collector contact layer. The base-collector depletion capacitance model represents the two regimes when the base-collector depletion layer is contained within the lightly doped collector and when the depletion layer extends into the highly doped contact layer (as in [10]). This capacitance C_{BC} is also attributed to both the intrinsic and extrinsic base regions (using the established X dependency). Hole storage in the emitter was assumed to be negligible in HBT's and the associated capacitance was omitted from the model. Charge-storage in the base-emitter space-charge region can be significant at low current levels

and empirical relationship of Grossman [10] was used to describe the associated capacitance C_{BEs} .

It is very important to distinguish clearly between the equivalent circuit element values corresponding to variations with dc bias (and varying temperature due to self-heating) and those corresponding to changes in the instantaneous values of voltages and currents occurring at a faster rate than the thermal time constant τ_{TH} (that is at a constant temperature). The former correspond to the change in small-signal element value as a function of bias and temperature, whereas the latter correspond to the instantaneous large-signal microwave values (where $f \gg 1/2\pi\tau_{TH}$ —that is, above 1 MHz for power devices). The latter parameters are evaluated at a constant temperature corresponding to the temperature at the dc bias point.

The simulator described here has been developed to model structures with multiple emitter, base and collector contacts, as depicted in Fig. 1, and can handle any configuration. The simulation divides the structure into a number of basic "cells" containing usually one or two emitter fingers. Each emitter finger "cell" is treated as a separate heat source, which determines the local temperature (for the immediately surrounding base-emitter and base-collector structures) and is solved as a separate electrical cell, coupled to the transistor contacts. The parasitic elements L_{Bpar} , L_{Cpar} , L_{Epar} , R_{Bpar} , R_{Cpar} and R_{Epar} , in Fig. 3, each represent a series inductance and resistance representing the connecting lines (and probe) parasitic elements (and are usually small for power devices). Parasitic capacitances C_{BEpar} , C_{BCpar} , and C_{CEpar} model the passive inter-contact capacitances. Capacitances C_{Bpad} , C_{Epad} , and C_{Cpad} model the pad capacitances of the base, emitter, and collector, respectively. The functional form and typical parameter values of the capacitances and resistances in the physics-based model are shown in Table II.

Self-heating generally has a more pronounced effect in GaAs/AlGaAs HBT's than in silicon BJT's because of the lower thermal conductivity of GaAs. Heat dissipation can be largely attributed to line sources and has a time constant τ_{TH} , typically in the region of a microsecond. A new model has been developed by the author to model the thermal properties of multicell HBT's. Liou *et al.* [22], [23] have shown that the variation in temperature between individual cells in HBT's can be significant and will eventually lead to thermal runaway and thermally triggered collapse of the collector current. The collapse of the collector current at high power densities occurs because of the negative temperature coefficient of the collector current and base-emitter voltage at constant base current. Liou's analysis is based on large-scale numerical solution of the thermal problem. This reveals very interesting and useful data, but is too slow for CAD and everyday usage. A thermal equivalent circuit-based approach was described by Baureis [24] who developed a multicell thermal model based on transforming measured inter-emitter temperature measurements to a thermal equivalent circuit with the interaction between each emitter described by thermal resistances coupling each emitter. In this way each emitter is considered as a thermal source interacting with every other emitter stripe.

TABLE II
FUNCTIONAL FORMS AND TYPICAL PARAMETER VALUES FOR CAPACITANCES AND RESISTANCES
FOR THE PHYSICS-BASED MODEL OF A $16 \times 3 \times 20 \mu\text{m}$ (16-EMITTER FINGER) TRANSISTOR

Model Element	Description and Comments	Functional Form	Typical parameter values per cell for $16 \times 3 \times 20 \mu\text{m}$ emitter HBT (2 emitter fingers/cell)
C_{BC}, C_{BE}	Base-collector and base-emitter depletion capacitances (both have similar functional forms - C_{BC} is shown here for brevity) Forward bias modelled using SPICE model [21].	$v_{BC} < 0 \quad C_{BC} \approx \left(\left(\frac{C_{JC}}{1 + \frac{v_{BC}}{V_{JC}}} \right)^{M_C} + C_{BCmm} \right) \frac{1}{N_C}$ $C_{JC} = A_C \sqrt{q \epsilon N_{Dcoll} N_{Abase} / (2 V_{JC} (N_{Abase} + N_{Dcoll}))}$ $V_{JC} = \frac{kT}{q} \ln(N_{Abase} N_{Dcoll} / n_i^2) + \delta E_{Ccoll}$	$N_C = 6$ $M_C = 0.5$ $M_E = 0.52$ $(M \approx 0.33 \text{ for lin. graded jn's})$ $V_{JC} = 1.4 \text{ V}, V_{JE} = 1.6 \text{ V}$ $A_C = \text{area of B-C junc.}$ $X = 0.25$ $n_i = \text{intrinsic carrier density}$ $\delta E_{Ccoll} = \text{collector conduction band discontinuity}$ $N_{Abase}, N_{Dcoll}, \text{base and intrinsic collector doping}$
C_{BEs}	Charge storage in base-emitter SCR.	$C_{BEs} = 0.5 C_{BEs0} \left(1 + \tanh \left(\frac{k_{BEs} (v_{BE} - F_{BE} V_{JE})}{V_{JE}} \right) \right)$	$C_{BEs0} = 8 \text{ fF}$ $F_E = 0.75$ $k_{BEs} = 18$
C_{BCH}	Diffusion capacitance (usually negligible)	$C_{BCH} = \frac{\tau_{CH}}{N_{BCH} V_{Ti}} I_{SBCH} \left(\exp \left(\frac{v_{BC}}{N_{BCH} V_{Ti}} \right) - 1 \right)$ (assumes a constant lifetime, I_{BCH} models hole inj. into base)	$\tau_{BCH} = 1 \text{ ns}$
$R_{Bcont}, R_{Ccont}, R_{Econt}$	Lateral contact resistances. NB: L is the contact length W is the width.	$R_{cont} = \sqrt{R_s / G_c} / \left(W \tanh \left(\frac{L}{L_c} \right) \right) \quad L_c = \sqrt{\frac{1}{G_c R_s}}$ R_s sheet resistance of layer, G_c contact conduct./unit area.	$R_{Bcont} = 3.54 \Omega$ $R_{Ccont} = 0.82 \Omega$ $R_{Econt} = 0.83 \Omega$ $W = 20 \mu\text{m}$ $L = 3 \mu\text{m}$ 2 fingers per cell
$R_{BExt}, R_{CEExt}, R_{EEExt}, R_{Cundepl}$	Bulk ohmic resistances. (again L is length and W width).	$R_{Ext} = R_s \frac{L}{W} \quad R_{Cundepl} = R_s \frac{(w_{coll} - w_c)}{L_c} \quad (w_c < w_{coll})$ $R_{Cundepl}$ is the resistance of the undepleted collector layer.	$R_{BExt} = 1.56 \Omega$ $R_{CEExt} = 0.69 \Omega$ $R_{EEExt} = 0.66 \Omega$ $R_{Cundepl} = 0 \text{ to } 3.4 \Omega \text{ (per cell)}$
R_{Econt}	Vertical emitter contact resistance	$R_{cont} = \frac{1}{A_{cont} G_c} \quad A_{cont} \text{ is contact area (metallization).}$	$R_{Econt} = 1.67 \Omega$ 2 fingers per cell
R_{BB}, R_{CC}	Base and collector spreading resistances. (equation is similar for both resistances)	$R_{spread} = \frac{R_s L}{K_{geom} W}$ $K_{geom} = 3$ for current entering from one side (single contact) $K_{geom} = 12$ for current entering from two sides (two contacts)	$R_{BB} = 1.76 \Omega$ $R_{CC} = 1.04 \Omega$ (values per cell)
$L_{Bpar}, R_{Bpar}, L_{Cpar}, R_{Cpar}, L_{Epar}, R_{Epar}$	Terminal parasitic inductance and resistance		$L_{Bpar} = 110 \text{ pH}, R_{Bpar} = 0.05 \Omega$ $L_{Cpar} = 100 \text{ pH}, R_{Cpar} = 0.03 \Omega$ $L_{Epar} = 70 \text{ pH}, R_{Epar} = 0.01 \Omega$
$C_{BEpar}, C_{BCpar}, C_{CEpar}$	Inter-electrode parasitic capacitances		$C_{BEpar} = 190 \text{ fF}$ $C_{BCpar} = 90 \text{ fF}$ $C_{CEpar} = 180 \text{ fF}$
$C_{Bpad}, C_{Cpad}, C_{Epad}$	Pad capacitances	$C_{pad} = \epsilon A_{pad} / s_{substrate}$ $s_{substrate}$ is substrate thickness, A_{pad}, pad area, ϵ permittivity.	$C_{Bpad} = 27 \text{ fF}$ $C_{Cpad} = 29 \text{ fF}$ $C_{Epad} = 23 \text{ fF}$

The multicell thermal analysis in this work is based on new thermal resistance matrix scheme. This can be understood by considering the two forms of thermal equivalent circuit for of a three emitter finger HBT shown in Fig. 5. It is possible to analyze a specific design of HBT using the type of equivalent circuit shown in Fig. 5(a) (as in [24]), which

is easy to interpret, but difficult to associate directly with a generalized characterization technique (this approach is closer to the idea of a thermal conductance matrix) and becomes increasingly topologically complex with increasing numbers of emitter fingers. However, a more generalized and flexible analysis can be based on the model shown in Fig. 5(b),

TABLE III
THERMAL RESISTANCE MATRIX FOR AN EIGHT-FINGER $8 \times 3 \times 20 \mu\text{m}$ AlGaAs/GaAs HBT, (EMITTER FINGERS ARE GROUPED ON CELLS OF TWO FINGERS), CALCULATED USING THE HEATWAVE 3-D THERMAL SIMULATOR

803.7	257.9	47.2	39.4	17.0	15.1	8.1	6.6
257.9	803.4	63.8	47.1	21.0	17.0	8.9	8.1
47.2	63.8	802.8	257.8	46.9	39.3	17.0	15.1
39.4	47.1	257.8	802.5	63.7	46.9	20.7	17.0
17.0	21.0	46.9	63.7	802.5	257.8	47.1	39.4
15.1	17.0	39.3	46.9	257.8	802.8	63.8	47.2
8.1	8.9	17.0	20.7	46.9	63.8	803.4	257.9
6.6	8.1	15.1	17.0	39.4	47.2	257.9	803.7

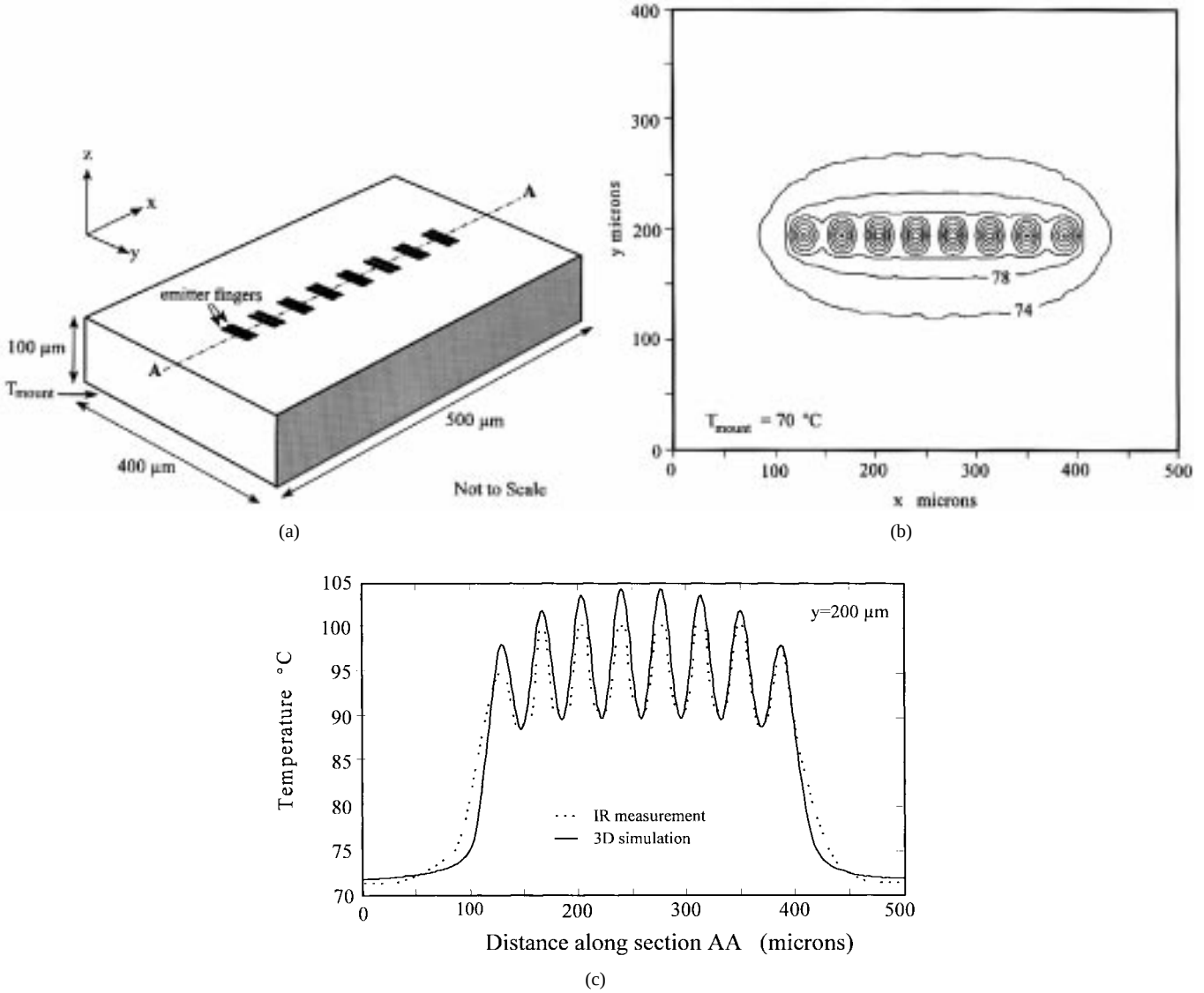


Fig. 6. Temperature distribution on the surface of a 16-finger ($16 \times 3 \times 20 \mu\text{m}$) emitter HBT, with emitter fingers group in subsets of two. (a) HBT layout showing schematic position of emitter fingers. (b) Contour plot of surface temperature of full chip device $0.4 \times 0.5 \text{ mm}$, contours are spaced 4°C apart with a die mounting temperature T_{mount} of 70°C . (c) Temperature profile at section AA across the HBT comparing simulated data with infrared measured data (resolution of IR measured data is 1.7°C).

which can immediately be associated with the concept of a thermal resistance matrix. This is conceptually slightly harder to visualise at first inspection as the elements *do not* correspond directly with equivalent circuit resistances of Fig. 5(a), but

are readily extracted from measured or simulated data, and the model is very easy to expand to devices with large numbers of emitter fingers. In fact, as we will see, the coupled thermal equivalent circuit resistances in Fig. 5(a) increase

with increasing cell separation, whereas the coupled thermal resistances in the matrix associated with Fig. 5(b) decrease in value with increasing separation.

Following the model topology of Fig. 5(b), the temperatures of the cells T are related to the power dissipated in each cell P defined by

$$[T - T_0] = [R_{Th}][P] \quad (3)$$

where the power dissipation P_i in each cell i is given by

$$P_i = V_{CB} \cdot I_{C_i} + V_{BE} \cdot I_{E_i}. \quad (4)$$

Note that in the multicell model the emitter and collector currents are all a function of the individual cells and the thermal interaction with associated cells. The thermal resistance matrix $[R_{Th}]$ is defined as in Fig. 5(b), by the matrix

$$[R_{Th}] = \begin{bmatrix} R_{11} & R_{12} & R_{13} & \cdots \\ R_{21} & R_{22} & R_{23} & \cdots \\ R_{31} & R_{32} & R_{33} & \cdots \\ \vdots & \vdots & \vdots & \ddots \end{bmatrix} \quad \text{where} \quad (5)$$

$$R_{ij} = \left. \frac{T_i - T_0}{P_j} \right|_{P_1 \cdots P_{j-1}, P_{j+1}, \dots, P_n = 0}.$$

Note that for the matrix entry i, j $R_{Thij} = R_{Thji}$ (i.e., $R_{Th12} = R_{Th21}$, $R_{Th13} = R_{Th31}$, etc). $P_1, P_2 \dots$ are the power dissipations in each respective finger. This leads to a matrix with some elements of symmetry. Also at low temperatures and as an initial estimate at low-moderate current densities $R_{Th33} = R_{Th11}$ (with similar symmetry for larger numbers of emitter fingers). However, it is important to appreciate that the whole matrix must be developed during the analysis because at high power densities it is possible for any one of the cells to experience thermal runaway (in which case $R_{Th33} \neq R_{Th11}$ etc). The thermal resistance matrix must be evaluated at each simulation point where the bias has changed as the thermal resistance element values R_{Thij} are a function of temperature. In this paper it is assumed that the temperature of the device is a function of the large-signal operating dc voltages and currents at the transistor terminals, as the microwave signal varies at a rate far higher than the thermal time constant.

In practice the self-induced thermal resistance R_{Thii} is usually close to the thermal resistance of an isolated single cell. The magnitude of the coupled thermal resistance R_{Thij} depends on the design of the transistor and in particular the separation. If the separation between cells is large then R_{Thij} tends to zero, and if the separation is very small its value tends to R_{Thii} . Hence, the coupled thermal resistance between distant cells is significantly smaller than the coupled thermal resistance of adjacent cells. In practice, the interaction between adjacent cells overwhelms the influence of other cells and errors in determining coefficients, other than those of closely coupled cells, have only minimal impact of the model.

The thermal resistances at a given average die temperature can be determined for test structures where individual emitter fingers are electrically isolated from adjacent fingers. The finger n is biased at an appropriate level, dissipating power P_n , and the temperatures of all the other unbiased fingers x

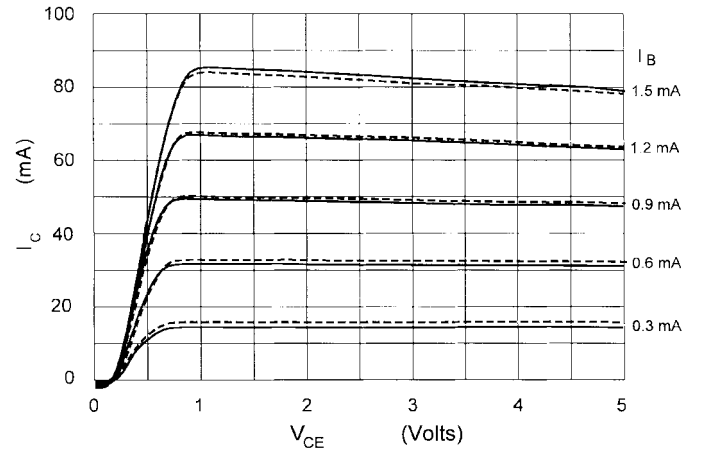


Fig. 7. Simulated and measured dc characteristics of a $16 \times 3 \times 20 \mu\text{m}$ emitter HBT (T_{mount} of 50°C).

are measured. In this way the thermal resistance matrix is calculated using $R_{nn} = (T_n - T_0)/P_n$ and $R_{xn} = (T_x - T_0)/P_n$ where $P_0 \cdots P_{n-1}, P_{n+1} \cdots P_N = 0$. This process is repeated $N/2$ times for an N finger transistor (symmetry), requiring $N/2$ test structures with electrically isolated fingers and can be carried out experimentally, using fabricated test structures (for example, as part of process monitor area of the wafer) or by utilizing a three-dimensional (3-D) thermal analysis simulator.

A 3-D thermal analysis simulation, *HeatWave*, was written to calculate the thermal resistance matrix using the highly efficient technique described in [22], [23], and [25]. The heat flow equation $\nabla \cdot \kappa(T) \nabla T = 0$ is solved for a 3-D temperature distribution using the method of Liou [22] and Gao *et al.* [25], utilizing the Kirchhoff transform for temperature-dependent conductivity, to yield the temperature distribution close to the surface (in the active region of the transistor). This method uses a double Fourier expansion method to speed up the solution. The heatsink is assumed to be attached to the bottom of the substrate (at $T = T_{\text{mount}}$), whilst all other surfaces except the heat sources (region below the emitter fingers) are assumed to be adiabatic. The model accounts for the heat-shunt effect of an airbridge. The test structures with isolated emitter stripes, described above, are simulated for the actual die size, for a given die mounting temperature. The matrix for a power HBT with 16 emitter fingers requires 16 separate thermal simulations, but can typically be extracted in 30 min on a personal computer, yielding a typical accuracy of better than 5% (when compared with results obtained from infrared measurement). A typical thermal resistance matrix for an eight-finger HBT (with emitter fingers grouped two per cell) obtained using this approach is shown in Table III. This approach avoids the need to perform an experimental temperature characterization of each design. The same simulator has been used to validate the thermal aspects of the electrothermal model by comparing the temperature distribution of the full simulated device with measured infrared data. A typical surface temperature distribution for an eight cell device with two closely spaced emitter fingers per cell (16 emitter fingers in total) is shown in Fig. 6. Note that it is not

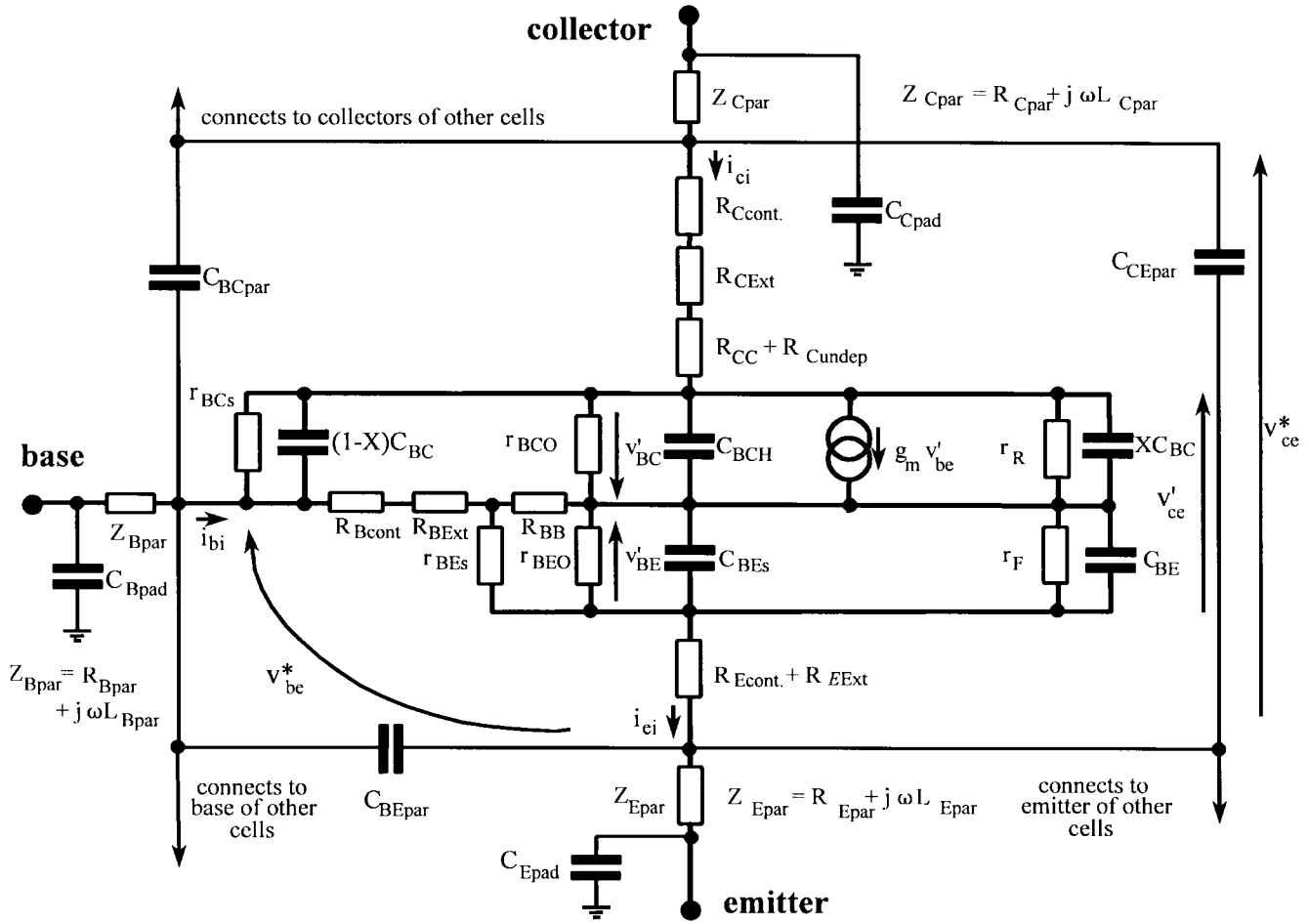


Fig. 8. Physics-based small-signal equivalent circuit model of HBT (active region).

possible to distinguish the temperature of individual emitter fingers in each cell because of their close proximity, although there is significant variation in temperature between cells (simulated at $V_{CE} = 4$ V $I_C = 0.25$ A, below current collapse or thermal runaway). The 3-D simulator *HeatWave* utilized over 13 300 mesh points on the surface of the device to obtain these results, achieving very good agreement with measured IR data, shown in Fig. 7 (note that the IR measurements have a resolution of 1.7 °C).

The electrothermal utilizes the thermal resistance matrix in conjunction with (4) and (5) to calculate the distributed temperatures, which are then used in self-consistent fashion with the physics-based electrical model to determine the instantaneous terminal currents and voltages. The thermal time constant τ_{TH} of the device is simulated using a simplified combination $R_{TH}C_{TH}$ where R_{TH} is the net thermal resistance of the device. In this paper the thermal time constant was measured for sample dies, for a given average die temperature (typical values were found to lie in the range 0.1 – 50 μ s). The thermal resistance (and the thermal resistance matrix element values) is a function of temperature and is approximated using

$$R_{TH} = R_{TH}(300) + \frac{dR_{TH}}{dT} \cdot (T - 300). \quad (6)$$

The rate of change of the thermal resistance with temperature was taken as 5 W^{-1} in this paper.

III. NUMERICAL SOLUTION

The HBT nonlinear equivalent circuit model is analyzed using a nonlinear nodal analysis routine, solving each emitter “cell” simultaneously. The nodal analysis proceeds by establishing the microwave equivalent circuit matrices such that

$$YV = I \quad (7)$$

where Y is the nodal admittance matrix and V and I are the nodal voltage and current vectors (dc or time-dependent), respectively. The current matrix I contains both linear and nonlinear sources. In the case of a solution scheme where the thermal model is not simultaneously solved directly with the electrical model, the matrices are re-arranged into the form

$$F = YV - I \quad \text{solving for } F = 0. \quad (8)$$

A modified Newton scheme was implemented to solve the nodal matrices using the scheme

$$F' \delta V = -F \quad (9)$$

where F' is the Jacobian (with entries $F'_{i,j} = \partial F_i / \partial V_j$) and δV is the vector of values $\delta V_j = V_j^{\text{new}} - V_j^{\text{old}}$. Here

$$F' = Y - I'. \quad (10)$$

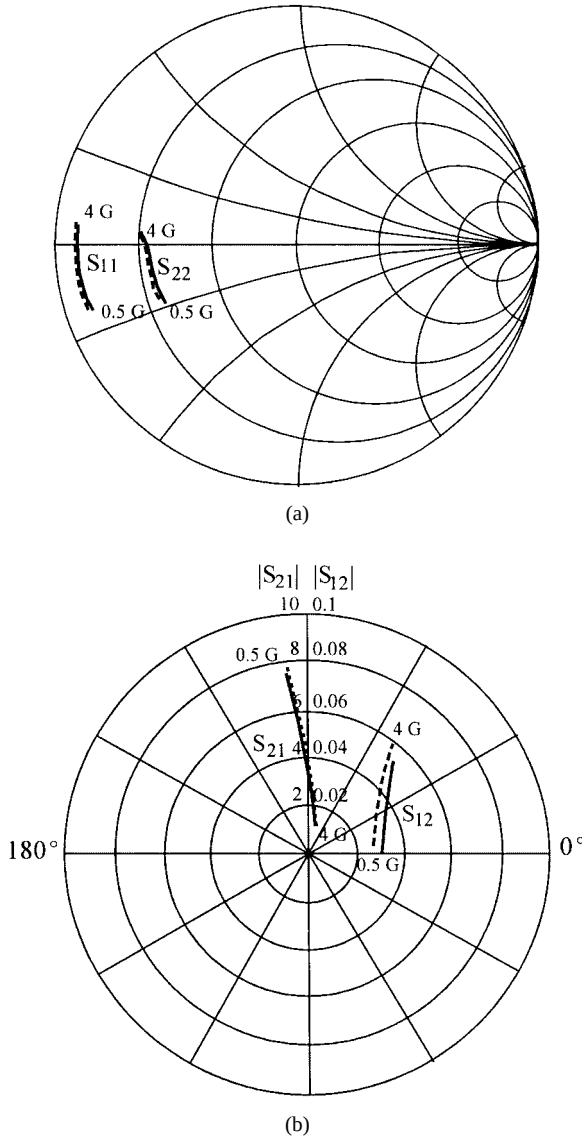


Fig. 9. S parameters of $16 \times 3 \times 20 \mu\text{m}$ emitter AlGaAs/GaAs HBT ($V_{CE} = 3 \text{ V}$, $I_C = 40 \text{ mA}$, $T_{\text{mount}} = 40^\circ\text{C}$). — simulated, - - - measured data.

Here the admittance matrix has been linearized. The implementation of this scheme results in an iterative scheme where each matrix is re-evaluated each iteration; the nonlinear admittance matrix elements being updated using values obtained with the most recent nodal voltage values. The updated nodal voltages are obtained using

$$\mathbf{V}^{\text{new}} = \mathbf{V}^{\text{old}} + \gamma \delta \mathbf{V}. \quad (11)$$

Note that a relaxation factor γ multiplies the vector $\delta \mathbf{V}$ in this scheme. This is essential to ensure convergence using the linearized admittance matrix in this nonlinear scheme. An adaptive system is used to select the optimum value of γ , based on the rate of convergence and the requirement, $\|\mathbf{F}^{\text{new}}\| < \|\mathbf{F}^{\text{old}}\|$. The use of modified Newton schemes is discussed in detail in [26]. A particularly effective algorithm for selecting the relaxation factor γ was developed during this

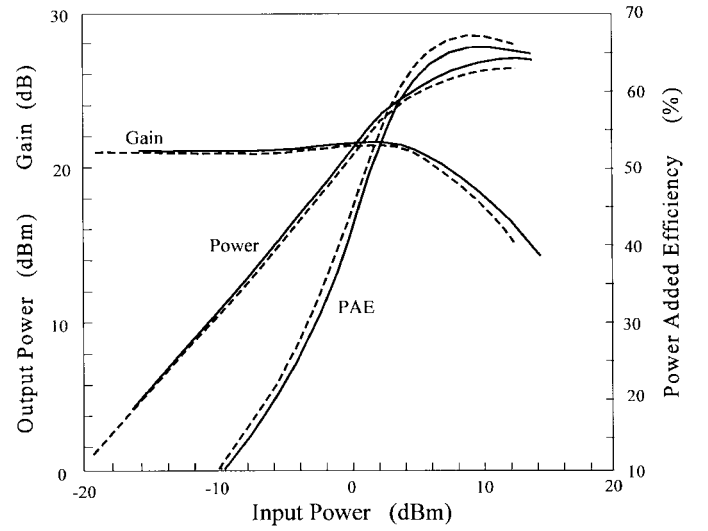


Fig. 10. Simulated and measured power transfer characteristics of $16 \times 3 \times 20 \mu\text{m}$ emitter AlGaAs/GaAs chip HBT ($V_{CE} = 4.2 \text{ V}$, $I_C = 40 \text{ mA}$, $T_{\text{mount}} = 60^\circ\text{C}$), operating in Class AB mode at 900 MHz, tuned for maximum power with $\Gamma_{\text{source}} = 0.75 \angle -175^\circ$, $\Gamma_{\text{load}} = 0.5 \angle 155^\circ$.

work and takes the form:

$$\gamma = \left| \left(\frac{1}{1 + V_{\text{max}} \xi_{\text{max}}} \right) \right| \quad (12)$$

where V_{max} is the maximum of the nodal voltages at that iteration and ξ_{max} is the maximum error at that iteration (δV_{max}). This algorithm allows stable convergence rates of up to 100 times faster than when using conventional means of determining the relaxation parameter [26].

This solution scheme involves the development of several large and complex matrices. The extraction of the Jacobian is particularly involved because of the inter-dependency of the current sources on several of the nodal voltages. However, once the scheme was coded it has proven to be robust and normally requires between 4 and 30 iterations to achieve convergence to 0.1 μV at every node in the model (i.e., typically $10^{-5}\%$).

The full electrothermal model can be solved for the system

$$\begin{bmatrix} \frac{\partial F_1}{\partial V} & \frac{\partial F_1}{\partial T} \\ \frac{\partial F_2}{\partial V} & \frac{\partial F_2}{\partial T} \end{bmatrix} \begin{bmatrix} \delta V \\ \delta T \end{bmatrix} = \begin{bmatrix} -F_1 \\ -F_2 \end{bmatrix} \quad (13)$$

where $\mathbf{F}_1 = \mathbf{YV} - \mathbf{I}$
 $\mathbf{F}_2 = \mathbf{R}_{TH} \mathbf{P}_{\text{diss}} - \Delta T$.

This system of equations is solved for $\mathbf{V}$ and $\mathbf{T}$ using an adaptive relaxation factor similar to (13). In practice the efficiency and convergence properties were found to be improved by solving the temperature dependence and thermal equations as a separate iterative loop (containing the above electrical solution) rather than performing a full nonlinear matrix solution. This approach is particularly expedient since the temperature solution is well behaved over most of the operating region of the device and convergence of the outer

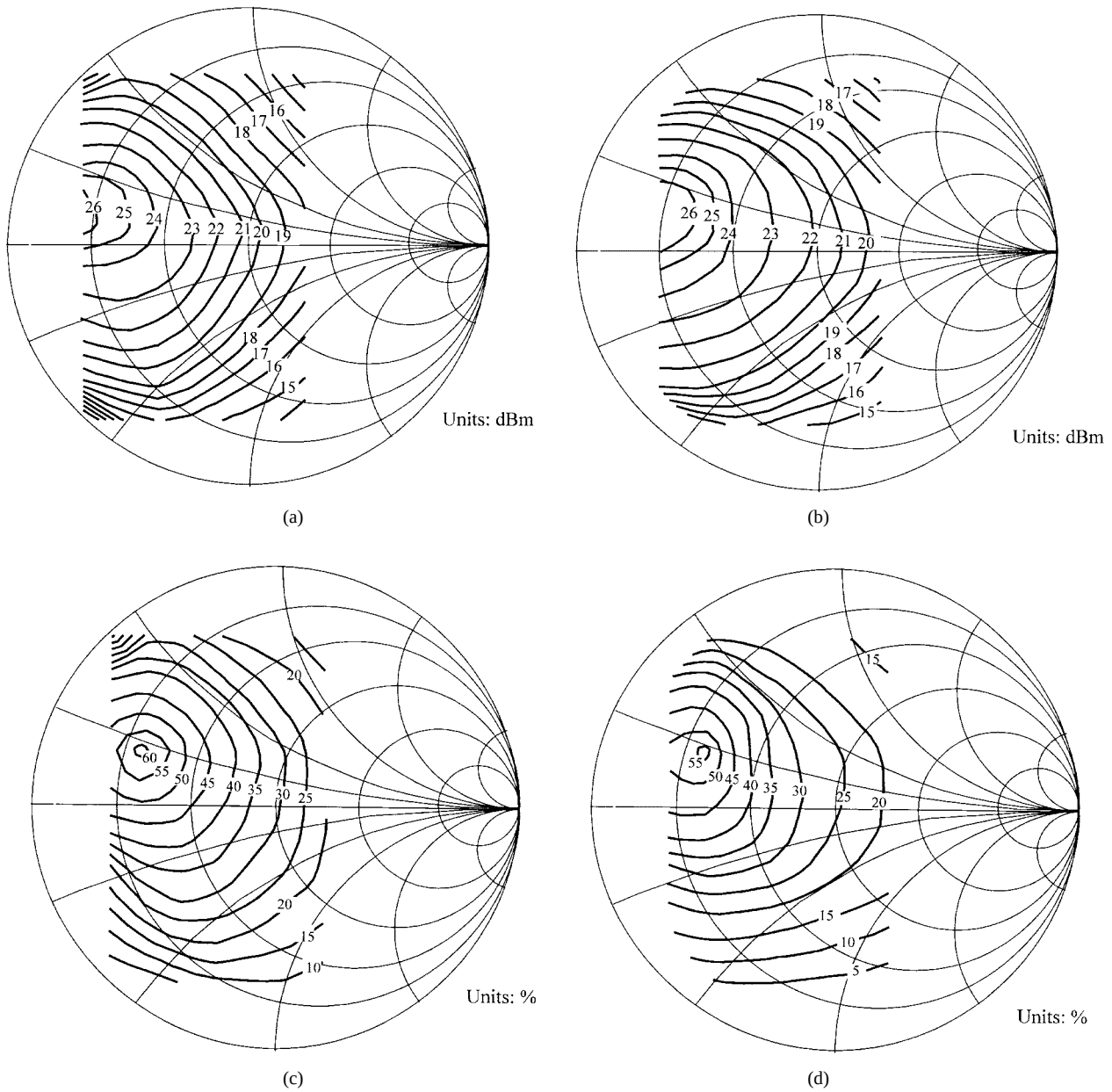


Fig. 11. (a) Simulated and (b) measured load-pull characteristics; (c) simulated and (d) measured power added efficiency characteristics as a function of impedance (at 1 dB compression point) of $32 \times 3 \times 20 \mu\text{m}$ emitter AlGaAs/GaAs HBT chip ($V_{CE} = 4.2 \text{ V}$, $I_C = 35 \text{ mA}$, $T_{\text{mount}} = 50^\circ\text{C}$), operating in Class AB mode at 1.88 GHz , $\Gamma_{\text{source}} = 0.8\angle -175^\circ$.

temperature loop occurs normally within two to three iterations (except during thermal runaway or current collapse when it may require up to ten iterations).

IV. DC SIMULATION RESULTS

The simulation has been used to model a variety of AlGaAs/GaAs and InGaAs/InP HBT's. Transistors consisting of 2, 8, and 16 emitter fingers and finally multicell devices with repeating sets of 16 fingers have been investigated. These larger power devices are of particular interest from the perspective of validating the model for large-signal purposes. Fig. 7 compares the measured and simulated results for dc characteristics of a $16 \times 3 \times 20 \mu\text{m}$ AlGaAs/GaAs HBT, for base currents in the range 0.3 to 1.5 mA at $T_{\text{mount}} = 45^\circ\text{C}$.

A current gain of 53 was obtained at $I_B = 1.5 \text{ mA}$ and $V_{CE} = 4 \text{ V}$. The simulation has been used to investigate current collapse at high power densities, arising from the nonuniform temperature distribution in the HBT.

V. SMALL-SIGNAL EQUIVALENT CIRCUIT MODEL AND S PARAMETERS

A small-signal equivalent circuit model is established by replacing the ideal diodes in the large-signal model with incremental resistances based on determining the small-signal incremental resistance of the diode at the bias-point

$$r_{\text{diode}} = \frac{\partial V_{\text{diode}}}{\partial I_{\text{diode}}} = \frac{NkT}{qI_s} \exp\left(\frac{-qV_{\text{diode}}}{NkT}\right) \bigg|_{V_{\text{diode}}}. \quad (14)$$

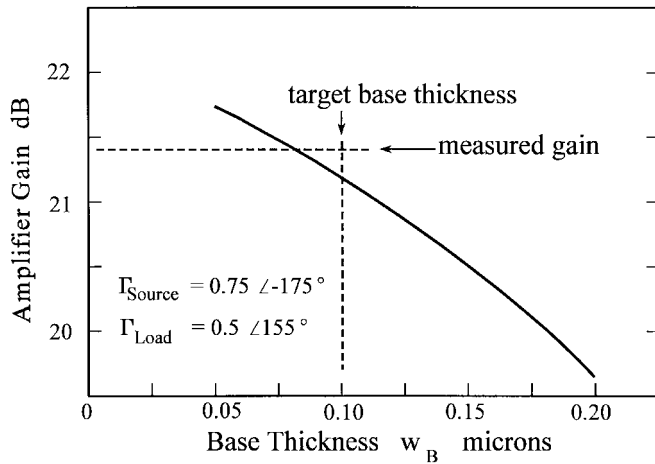


Fig. 12. Variation of amplifier gain as a function of base layer thickness for a 0.5-W power amplifier utilizing a $16 \times 3 \times 20 \mu\text{m}$ emitter AlGaAs/GaAs chip HBT ($V_{CE} = 4.2 \text{ V}$, $I_C = 40 \text{ mA}$, $T_{\text{mount}} = 40^\circ\text{C}$), at 900 MHz, with $\Gamma_{\text{source}} = 0.75 \angle -175^\circ$, $\Gamma_{\text{load}} = 0.5 \angle 155^\circ$.

This leads to a small-signal circuit model of the form shown in Fig. 8, which can be evaluated in the frequency domain. The resistances and capacitances of this model are obtained from the physical bias-dependent relationships. Steady-state small-signal CW operation is assumed in this model and the time-independent thermal model is utilized here.

The S parameters of an HBT are calculated using the bias-dependent small-signal equivalent circuit model. A dc simulation is performed to calculate the temperature of the device and establish the dc currents and voltages for the model. The bias-dependent element values are calculated to provide the data for the small-signal equivalent circuit model. The equivalent circuit model is analyzed to extract the nodal admittance matrix using a generalized algorithm. The admittance matrix is calculated at each frequency and then reduced to a 2×2 matrix using a pivotal condensation technique. The two-port admittance matrix is then converted in to a two-port S parameter matrix. This approach leads to a faster solution for small-signal parameters than the alternative time-domain simulation with the large-signal model.

It should be noted that the S parameters are a function of bias-point and ambient temperature. The comparison of a typical set of measured and simulated S parameter data is shown in Fig. 9 for $I_C = 40 \text{ mA}$ and $V_{CE} = 3 \text{ V}$. The transistors were measured using coplanar on-wafer probes with a HP8510C network analyzer, calibrated using LRM and an impedance standard substrate. It is also possible using this model to extract S parameters over the entire dc operating range for a constant given ambient temperature and requires only a matter of seconds on a workstation. This scenario corresponds to data extracted using pulse- S -parameter methods and could be utilized in conjunction with other large-signal design methods.

VI. LARGE-SIGNAL SIMULATION

Large-signal simulation is performed using a harmonic-balance scheme, which allows the harmonic performance of Class A, AB and B HBT amplifiers to be assessed. Steady-

state CW operation is assumed, utilizing the time-independent thermal model in conjunction with the large-signal model of Fig. 3. The harmonic-balance scheme is based on a secant-solver algorithm, which is computationally more efficient than traditional Jacobian schemes for small workstations and personal computers. The input and output load reflection coefficients are specified and the bias point is chosen by the user for a given die-mounting temperature. The simulator then performs a dc simulation to establish the initial bias and thermal conditions under small-signal conditions. This is followed by a number of simulations at varying power levels, starting at small signal conditions, where the power level at the input is steadily increased in steps until power saturation occurs at the output. The dc bias and temperature distribution are re-evaluated at each new increasing input signal level, modifying the dc nodal voltages, microwave performance and the temperature as the transistor operates in an increasingly nonlinear fashion. The harmonic-balance scheme tests for convergence by checking the time-domain voltage waveforms at the input and output for convergence over a number of iterations and testing for the rms error (with a minimum of $10 \mu\text{V}$ accuracy normally available). This is carried out in conjunction with a test for convergence in the input and output reflection coefficients to within an error of 0.02.

The large-signal performance of a $16 \times 3 \times 20 \mu\text{m}$ emitter AlGaAs/GaAs HBT operating at 900 MHz as a Class AB amplifier is shown in Fig. 10 (tuned for maximum output power), with simulated and measured data $I_C = 40 \text{ mA}$, $V_{CE} = 4.2 \text{ V}$, $T_{\text{mount}} = 60^\circ\text{C}$. When T_{mount} was varied from 40°C to 90°C the small-signal gain decreased by 1.5 dB and the P_{1dB} decreased by 1.8 dBm (measured and simulated data tracked closely). The load-pull characteristics for a larger $32 \times 3 \times 20 \mu\text{m}$ emitter device are shown in Fig. 11, illustrating the output power and power-added efficiency at the 1 dB compression point $I_C = 35 \text{ mA}$, $V_{CE} = 4.2 \text{ V}$, $T_{\text{mount}} = 50^\circ\text{C}$. The agreement between measured and simulated data is good, with deviations in the region of 1 dB and 5% PAE over the range of impedance investigated.

VII. MODELING PARAMETER SPREADS

Physical and physics-based models allow device and circuit parameter spreads due to variations in processing and wafer growth to be evaluated. The model described here has been used to investigate the impact of variation in the thickness and doping levels of the emitter, base and collector layers of the device. Fig. 12 shows the variation in amplifier gain for a 0.5-W 900 MHz HBT amplifier design as a function of base layer thickness. It is interesting to note that for an expected layer thickness of $0.1 \mu\text{m}$, the corresponding measured gain was 21.4 dB for the specified load and source reflection coefficients (at a mounting temperature of 40°C). The model predicts a gain of 21.1 dB for this base thickness, with a spread in gain of 2 dB as the thickness was varied from 0.05 to $0.2 \mu\text{m}$. This model allows designers to rapidly evaluate the spread in microwave and dc parameters as a function of geometry and layer specification, and is thus particularly suited to process-oriented design.

VIII. CONCLUSIONS

A comprehensive electrothermal model has been described which incorporates a physics-based equivalent circuit model and a new multifinger thermal model. A thermal resistance matrix method has been described which allows the rapid evaluation of the temperature distribution across the emitter fingers. The model has been validated for a variety of power HBT structures and has demonstrated good agreement for dc, small- and large-signal operations over a variety of operating conditions and die temperatures. This model is well suited to process-oriented CAD.

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